REMARKS/ARGUMENTS

Claims 44, 48, 49, and 60-68 are currently pending, of which claims 44, 61, and 65 are the independent claims. Claims 1-43, 45-47, and 50-59 were previously cancelled. No new claims are added herein, and no claims are amended or cancelled herein. No new matter is believed to have been introduced to the application by this paper. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC § 103

Claims 44, 48, 49, and 60-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U. S. Pat. No. 6,476,499 ("Hikita") in view of JP405123237A ("Shimizu"). Claims 48, 49, and 60-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hikita in view of Shimizu, and further in view of the Flip Chip Ball Grid Array (FPBGA) Package Family reference ("Flip Chip"). Claims 44, 48, 49, 60, 62-64, and 66-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over U.S. Pat. No. 5,894,172 ("Hyozo") in view of Shimizu, and further in view of Flip Chip. Claims 44, 48, 49, and 60-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hikita in view of JP362169448A ("Hiromasa"). Claims 48, 49, and 60-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hikita in view of Hiromasa, and further in view of Flip Chip. Claims 44, 48, 49, 60, 62-64, and 66-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hyozo in view of Hiromasa, and further in view of Flip Chip. Claims 65-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hikita in view of Hiromasa, and further in view of Shimizu. Claims 65-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hikita in view of Hiromasa, further in view of Flip Chip, and further in view of Shimizu. Claims 65-68 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hyozo in view of Hiromasa, further in view of Flip Chip, and further in view of Shimizu. Reconsideration and withdrawal of these rejections are respectfully requested.

Independent Claim 44 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. An identity of product is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said

multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said identity of product. The identity of product is visible through said optically transparent layer.

Independent Claim 61 relates to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. An identity of manufacturer is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said identity of manufacturer, wherein said identity of manufacturer is visible through said optically transparent layer.

Independent Claim 65 is directed to a circuit component comprising a substrate and a semiconductor chip over a top surface of said substrate. The semiconductor chip has a front surface facing said top surface of said substrate and a back surface opposite said front surface. The semiconductor chip comprises multiple pads at said front surface. A bar code is directly on said back surface of said semiconductor chip. Multiple metal bumps are between said multiple pads of said semiconductor chip and said top surface of said substrate. An optically transparent layer is vertically over said bar code. The bar code is visible through said optically transparent layer.

The applied references, either alone or in combination, are not seen to teach or suggest the foregoing combination of features of each of independent Claims 44, 61, and 65.

The Office Action states that it would have been obvious to one of ordinary skill in the art to "combine the teachings of Hikita et al. with those of Shimizu," (*See* Office Action, p. 3), and "to combine the teachings of Hikita et al. with those of Hiromasa." *See* Office Action, p. 8. Applicants respectfully disagree.

Hikita generally relates to "*a chip-on-chip structure in which semiconductor chips are bonded to each other in a face-to-face stacked relation, the semiconductor chip comprising an informational notation specific thereto provided on a back face thereof to be utilized at least when the chip-on-chip structure is assembled.*" *See* Hikita, col. 7, ll. 27-33. Hikita discloses

"*chip-on-chip semiconductor device is molded and then delivered to the market and, when a need arises to check makers and the like of the respective semiconductor chips incorporated in the semiconductor device, the back faces of the semiconductor chips are exposed from a mold package for checking the specific informational notations of the semiconductor chips. See* Hikita, col. 8, ll. 23-30. Thus, Hikita discloses that the chip-on-chip semiconductor device is molded such that under normal operation the informational notations of the semiconductor chips are not exposed, and therefore are protected from damage resulting from long periods of exposure, e.g. wear, scratches, and erasing. Hikita further discloses that after assembly, only under specific circumstances is the back face of the semiconductor chip exposed from the mold package to expose the informational notation. *See* Hikita, col. 8, ll. 23-30. Thus, there is no motivation, or need, to apply the resin of Shimizu, or the film of Hiromasa, to Hikita's semiconductor chips, because the informational notation of Hikita is normally protected by the mold package and therefore not exposed during operation and/or storage. Furthermore, Applicants respectfully submit that after Hikita's semi-conductor device is assembled, the informational notation would likely be marked on a package, such as the package 2 disclosed in Hiromasa. The informational notation would then be referenced by viewing the package 2, instead of by exposing the back face of the chip from the otherwise closed mold packaging.

Shimizu generally relates to "*providing a bar-code or a matrix code being fit for a long period of use on the side face or the bottom face of tableware.*" *See* Shimizu, p. 1. Shimizu discloses "*a prescribed resin member is printed or applied by superimposing it on the bar codes 3A, 3B for the purpose of wear resistance or scratch resistance or water resistance.*" *See* Shimizu, pp. 1-2. Thus, Shimizu discloses applying a resin member on tableware for the purpose of protecting an exposed bar code from damage that may occur from a long period of exposure, i.e. wear, scratches, etc. However, as previously discussed, Hikita discloses an informational notation which is normally not exposed in operation and/or storage, and therefore is normally protected from damage that occurs over a long period of exposure, e.g. wear, scratches, etc. Assuming, in arguendo, that Hikita's informational notation were exposed during an inspection, any such exposure would be infrequent, and over a short period of time, not over a long period of time such as during operation and/or storage. Thus, Applicants respectfully submit that there is no objective motivation, or need, to combine Shimizu's teaching of using a resin to protect against damage resulting from long periods of exposure with Hikita's informational notation and

mold package, because the informational notation of Hikita is already protected from damage resulting from long periods of exposure by the mold package. Furthermore, even when Hikita's informational notation may be exposed during an inspection, any such exposure would be infrequent and brief, and would not provide motivation to combine the informational notation and mold package of Hikita with Shimizu's teaching of protecting from exposure over long periods of time.

Applicants respectfully submit that since the informational notation of Hikita is normally not exposed for long periods of time, there is no objective motivation, or need, to apply Shimizu's teaching of using a resin to protect from long periods of exposure. Thus, there is no teaching, suggestion, or motivation to combine the resin of Shimizu with the informational notation and mold package of Hikita.

Hiromasa generally relates to a mark on the surface of a package where "*a film through which the mark and the like can be visually observed is provided thereon.*" *See* Hiromasa, p. 1. Hiromasa discloses "*[a]s a result, the degree of erasing of the letter, marks and the like can be reduced.*" *See* Hiromasa, p. 1. Thus, Hiromasa discloses applying a film to a package for the purpose of reducing the degree of erasing letters/marks resulting from excessive exposure due to the fact that the letters/marks on the package are always exposed. However, as previously discussed, Hikita discloses an informational notation which is normally not exposed, and therefore is normally protected from erasing. Thus, Applicants respectfully submit that there is no objective motivation, or need, to combine Hiromasa's teaching of using a film to protect against erasing resulting from excessive exposure, with Hikita's informational notation and mold package, as the informational notation of Hikita is already protected from erasing by the mold package. Furthermore, even when Hikita's informational notation may be exposed during an inspection, any such exposure would be brief and infrequent, and would not motivate one to combine the informational notation and mold package of Hikita with Hiromasa's teaching of protecting against erasing resulting from excessive exposure.

Applicants respectfully submit that since the informational notation of Hikita is normally not exposed for long periods of time, there is no objective motivation, or need, to apply Hiromasa's teaching of using protective film to protect from erasing resulting from excessive

exposure. Thus, there is no teaching, suggestion, or motivation to combine the film of Hiromasa with the informational notation and mold package of Hikita.

The Office Action states "*[t]he mere fact that Hikita's information is exposed is ample motivation to protect it from damage/alteration, as it is being inspected.*" Office Action, p. 15. Applicants respectfully disagree. Hikita's informational notation is not exposed during normal operation and is therefore normally protected against damage/alteration. Since Hikita's informational notation is normally protected against damage/alteration, there is no motivation, or need, to add a protective coating to Hikita's informational notation. Regardless, the cited references of Shimizu and Hiromasa teach adding a protective coating to protect from damage resulting from long periods of exposure, e.g. wear, erasing, etc. However, Hikita's informational notation is only exposed for brief periods of time during infrequent inspections, i.e. "*when the need arises to check makers and the like of the respective semiconductor chips*." *See* Hikita, col. 8, ll. 24-30. Thus, there is no motivation to combine Shimizu's, or Hiromasa's, teaching of protecting from long periods of exposure with Hikita's informational notation, because Hikita's informational notation is only subject to short, and infrequent, periods of exposure, and Hikita's informational notation is already protected from long periods of exposure.

The other applied references, Flip Chip and Hyozo, are not seen to cure the above-discussed deficiencies of Hikita, Shimizu and Hiromasa.

For the reasons discussed above, Claims 44, 61, and 65 are believed to be allowable over the applied references. Accordingly, reconsideration and withdrawal of the rejections of Claims 44, 61 and 65 are respectfully requested.

The other claims currently under consideration in the application are dependent from their respective independent claims discussed above and therefore are believed to be allowable over the applied references for at least similar reasons. Because each dependent claim is deemed to define an additional aspect of the invention, the individual consideration of each on its own merits is respectfully requested.

The absence of a reply to a specific rejection, issue, or comment does not signify agreement with or concession of that rejection, issue, or comment. In addition, because the arguments made above may not be exhaustive, there may be other reasons for patentability of any

or all claims that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment or cancellation of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment or cancellation.

CONCLUSION

In view of the remarks set forth herein, Applicant submits that the claims are in condition for allowance and respectfully requests a notice to this effect. Should the Examiner have any questions, please call the undersigned at the phone number listed below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

/Dennis A. Duchene/
Dennis A. Duchene
Registration No. 40,595

11682 El Camino Real, Suite 400
San Diego, CA 92130
Phone: 858.720.3300 MGD:asc
Facsimile: 858.720.7800
Date: October 25, 2010

Please recognize our Customer No. 89518 as our correspondence address.

Appendix - Related Cases Status

Docket Number	Serial Number	Filing Date	Examiner Name	Status
085027-0026	09/523,990	3/13/2000	WALSH, DANIEL I.	Final OA mailed 6/23/10
085027-0386	12/260,086	10/28/2008	WALSH, DANIEL I.	Final OA mailed 8/2/10